

● General Description

It combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$.

● Features

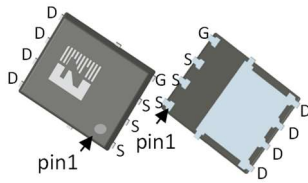
- Low $R_{DS(ON)}$ to minimize conductive loss
- Low Gate Charge for fast switching
- Low thermal resistance
- AEC-Q101 qualified

● Application

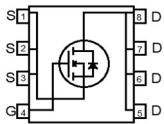
- BLDC motor driver
- DC-DC
- Battery protection



● Product Summary



DFN5*6



$V_{DS}=40V$

$R_{DS(ON)}=5.5m\Omega$

$I_D=68A$



● Ordering Information

Part NO.	ZMSA055N04HN
Marking	ZMS055N04H
Packing information	REEL TAPE
Basic ordering unit (pcs)	3000

● Absolute Maximum Ratings ($T_A=25^\circ C$, unless otherwise specified)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Drain-source voltage	V_{DS}		-	40	V
Gate-source voltage ^①	V_{GS}		-20	20	V
Continuous drain current	I_D	$V_{GS}=10V, T_C=25^\circ C$	-	68	A
	I_D	$V_{GS}=10V, T_C=75^\circ C$	-	63	A
	I_D	$V_{GS}=10V, T_C=100^\circ C$	-	55	A
Pulsed drain current ^①	I_{DM}	Pulsed; $t_p \leq 10 \mu s; T_C = 25^\circ C$;	-	272	A
Total power dissipation	P_D	$T_C=25^\circ C$	-	71	W
Total power dissipation	P_D	$T_A=25^\circ C$	-	3	W
Operating junction temperature	T_J		-55	175	$^\circ C$
Storage temperature	T_{STG}		-55	175	$^\circ C$
Single pulse avalanche energy	E_{AS}	$L=0.1mH, V_{GS}=10V, R_g=25\Omega$,	-	40	mJ
		$L=0.5mH, V_{GS}=10V, R_g=25\Omega$,	-	84	mJ
ESD level (HBM)			CLASS 1C		

● Thermal Resistance

Parameter	Symbol	Min.	Typ.	Max.	Unit
Thermal resistance, junction - case	R_{thJC}	-	-	2.1	°C/W
Thermal resistance, junction - ambient ^②	R_{thJA}	-	-	50	°C/W
Soldering temperature(total time<10s)	T_{sold}	-	-	260	°C

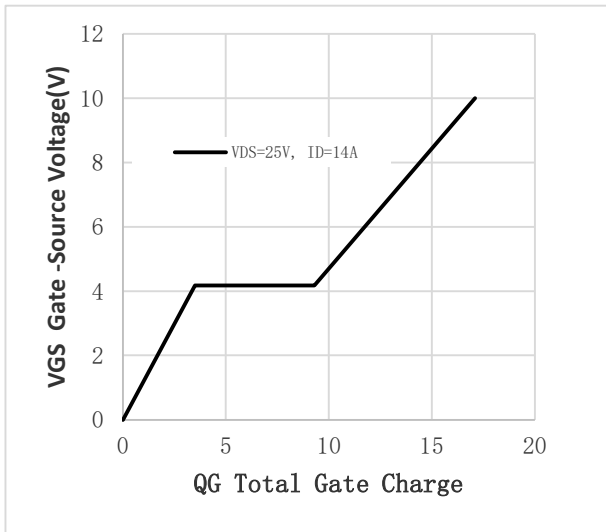
● Electronic Characteristics ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu A$	2	2.7	3.5	V
Drain-source leakage current	I_{DSS}	$V_{GS}=0V, V_{DS}=40V$	-	-	1	μA
Gate- source leakage current	I_{GSS}	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	100	nA
Static drain-source on resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=14A, T_j=25^{\circ}\text{C}$	-	5.5	6	m Ω
Forward transconductance	g_{FS}	$V_{DS}=5V, I_{SD}=4A$	-	7	-	S
Diode forward voltage	V_{FSD}	$V_{GS}=0V, I_{SD}=14A$	-	-	1.3	V

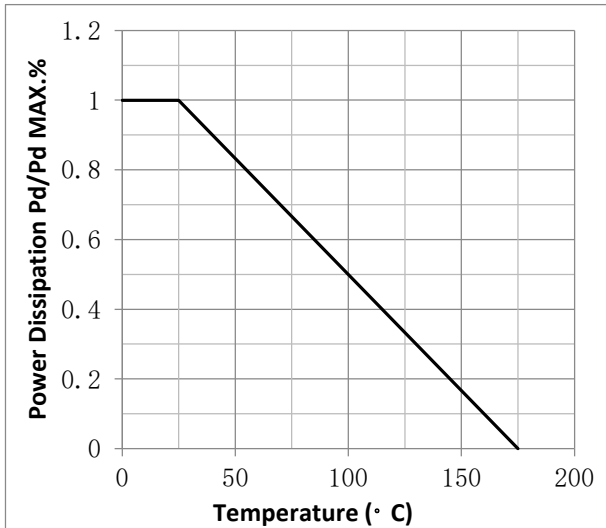
● Dynamic Characteristics ($T_j=25^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input capacitance	C_{iss}	$f=1\text{MHz}, V_{DS}=25V, V_{GS}=0V$	-	908	-	pF
Output capacitance	C_{oss}		-	244	-	pF
Reverse transfer capacitance	C_{rss}		-	10	-	pF
Gate resistance	R_g	$f=1\text{MHz}$	-	1.2	-	Ω
Total gate charge	Q_g	$V_{DD}=25V, I_D=14A, V_{GS}=10V$	-	17.1	-	nC
Gate-source charge	Q_{gs}		-	3.5	-	nC
Gate-drain charge	Q_{gd}		-	5.8	-	nC
Turn-on delay time	$t_{D(on)}$	$V_{GS}=10V, V_{DS}=15V, R_G=3.3\Omega, I_D=20A$	-	5	-	ns
Turn-on rise time	t_r		-	10	-	ns
Turn-off delay time	$t_{D(off)}$		-	8	-	ns
Turn-off fall time	t_f		-	3	-	ns
Reverse recovery time	t_{rr}	$V_{DD}=20V, di_s/dt=100A/\mu s, I_s=50A$	-	30	-	ns
Reverse recovery charge	Q_{rr}		-	21	-	nC

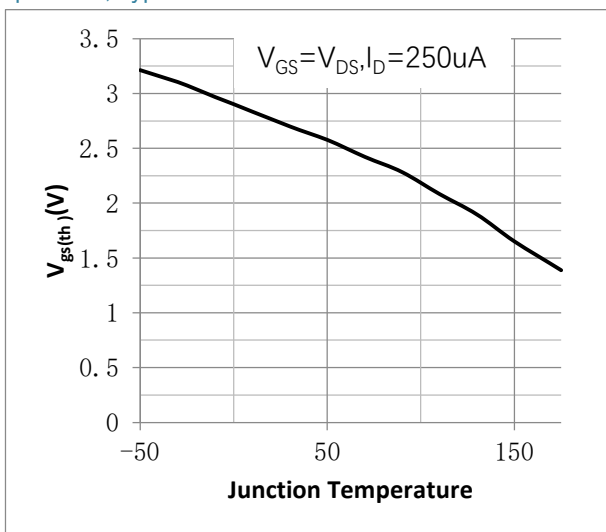
● Fig.1 Gate-source voltage as a function of gate charge; Typical values; $T_J=25^\circ\text{C}$



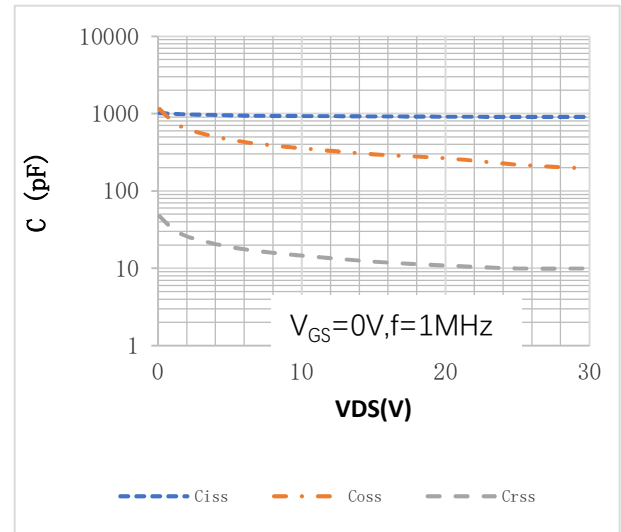
● Fig.3 Normalized total power dissipation as a function of case temperature; Calculative values Normalized Power Dissipation $=P_d/P_d(25^\circ\text{C})$



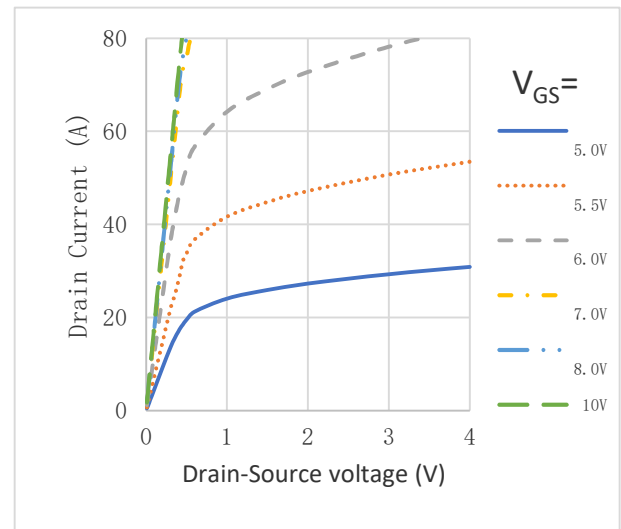
● Fig.5 Gate-source threshold voltage as a function of junction temperature; Typical values



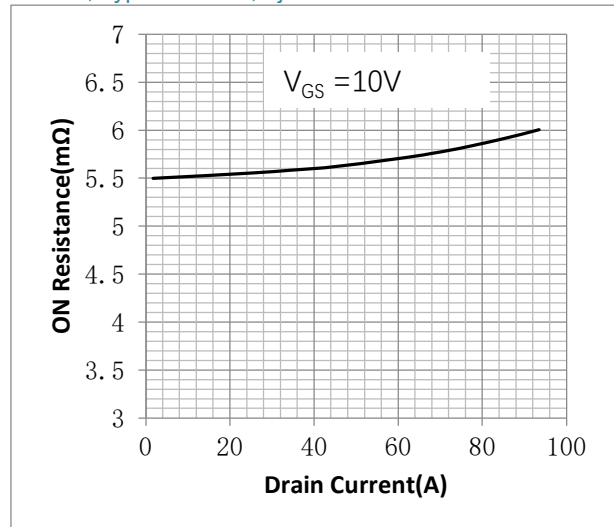
● Fig.2 Input, output and reverse transfer capacitances as a function of drain-source voltage; Typical values; $T_J=25^\circ\text{C}$



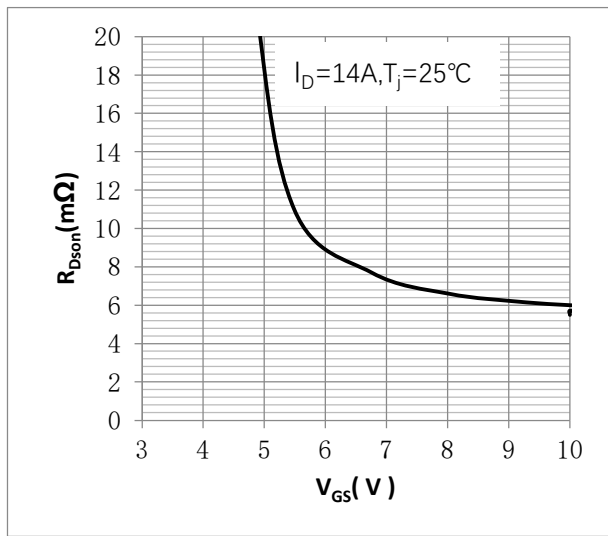
● Fig.4 Output characteristics: drain current as a function of drain-source voltage; Typical values; $T_J=25^\circ\text{C}$



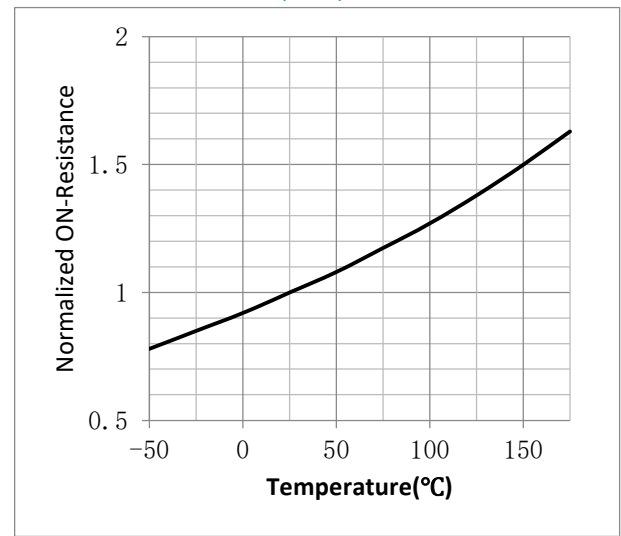
● Fig.6 Drain-source on-state resistance as a function of drain current; Typical values; $T_J=25^\circ\text{C}$



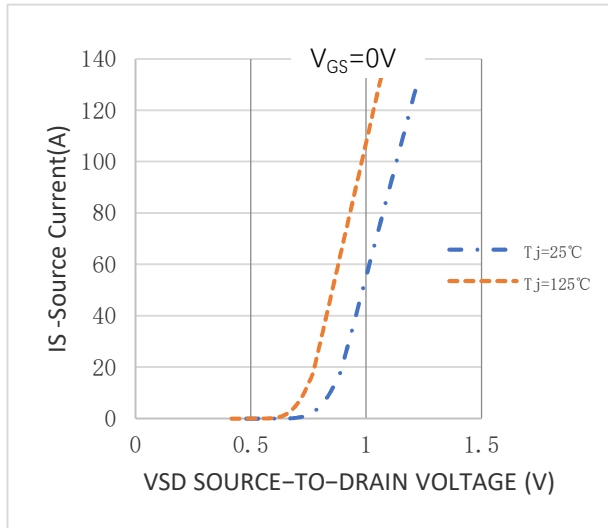
● Fig.7 Drain-source on-state resistance as a function of gate-source voltage; Typical values



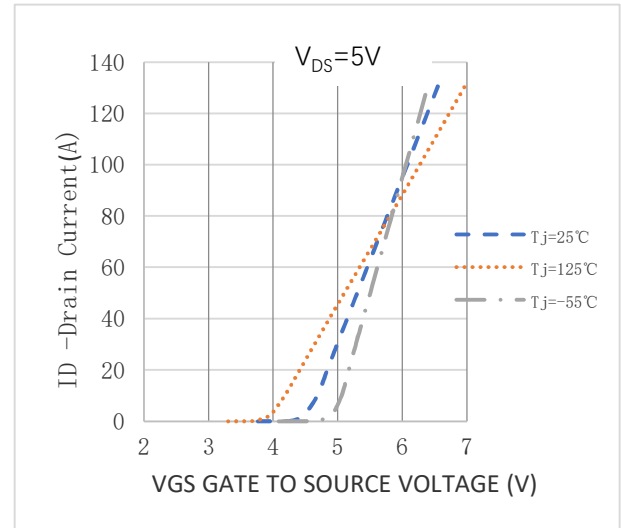
● Fig.8 Normalized drain-source on-state resistance factor as a function of junction temperature; Typical values Normalized On-Resistance= $R_{DS(on)}/R_{DS(on)}(25^\circ C)$



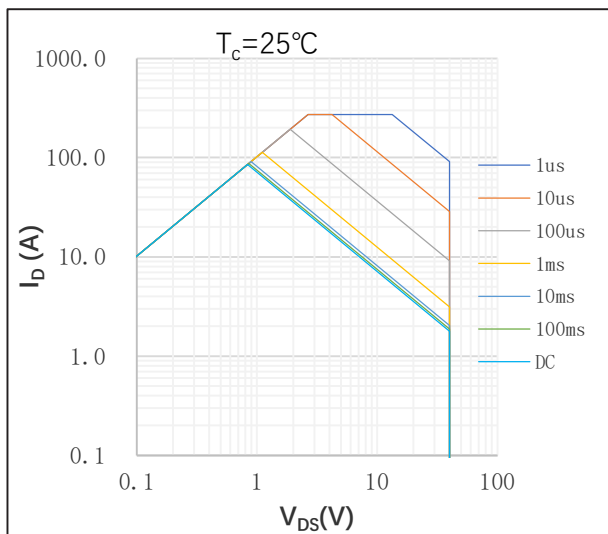
● Figure 9. Source (diode forward) current as a function of source-drain (diode forward) voltage; Typical values



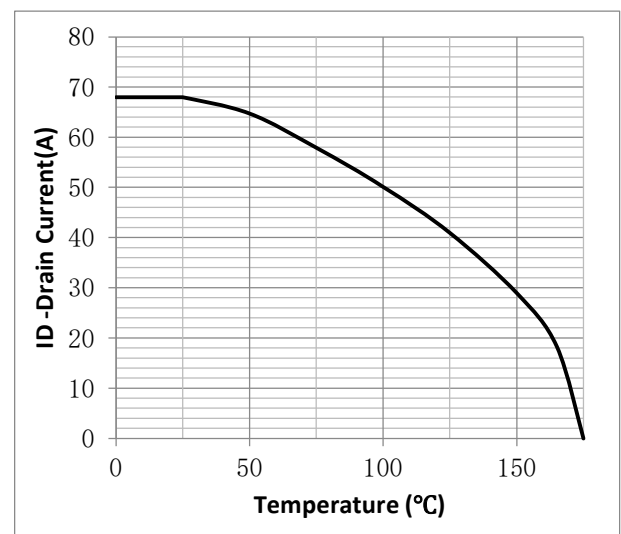
● Figure 10. Transfer characteristics: drain current as a function of gate-source voltage; Typical values



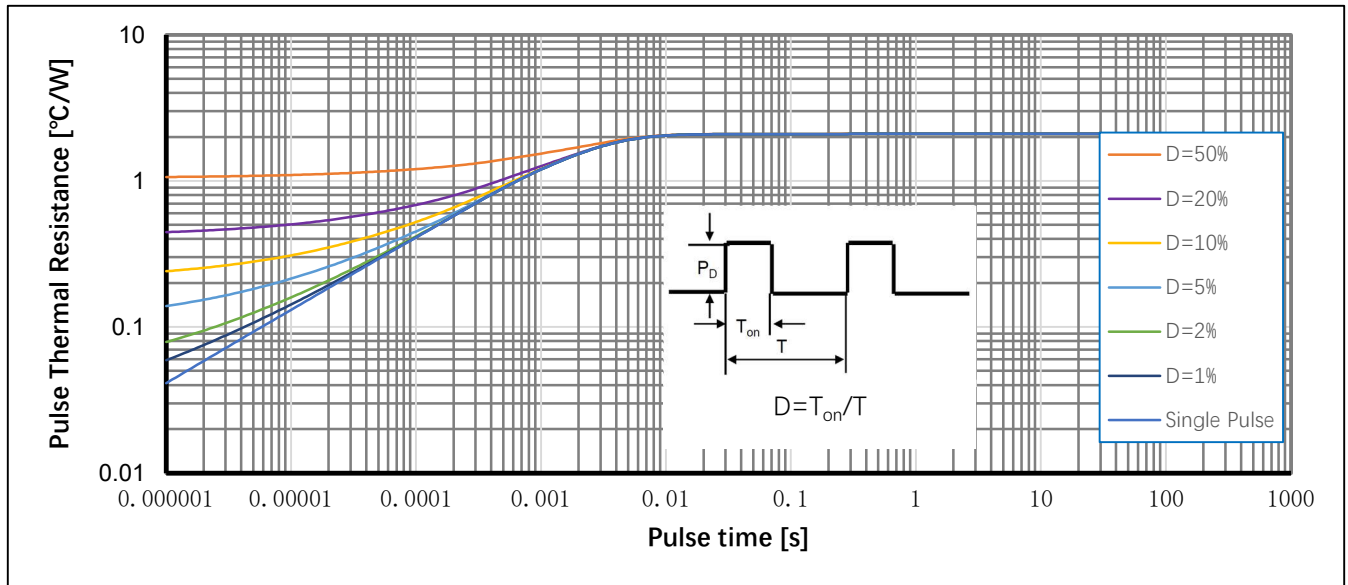
● Fig.11 Safe operating area: continuous and peak drain currents as a function of drain-source voltage; Calculative values



● Fig.12 Continuous drain current as a function of case temperature³; Calculative values

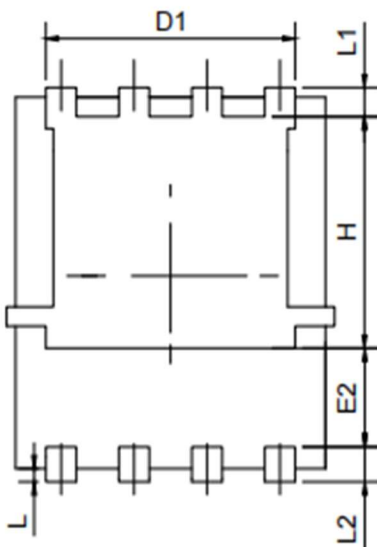
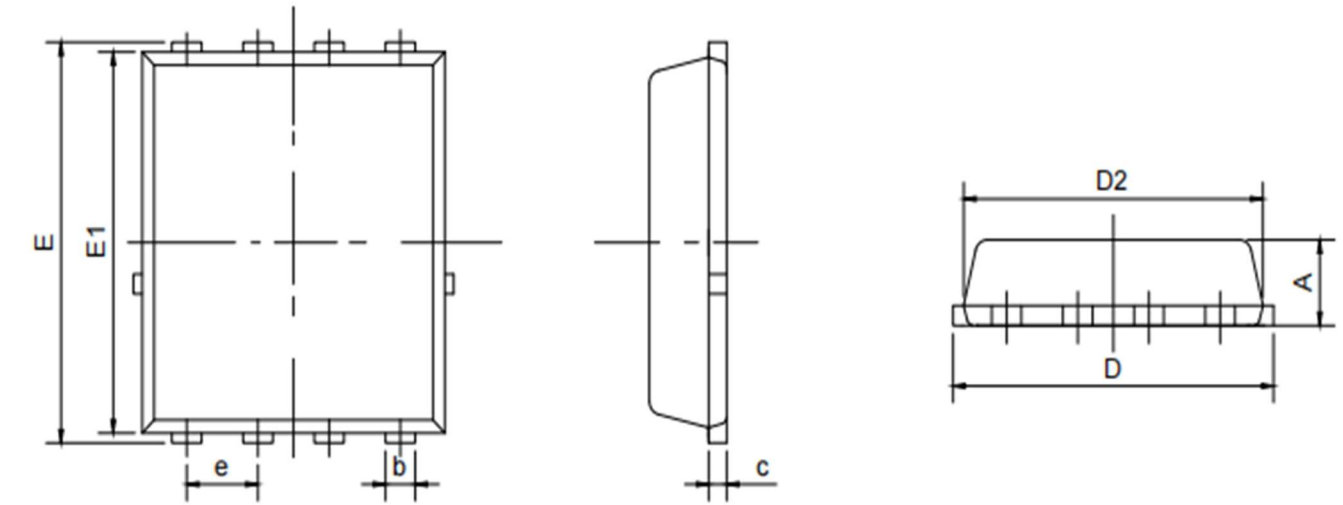


● Fig.13 Transient thermal impedance from junction to case as a function of pulse duration; max values

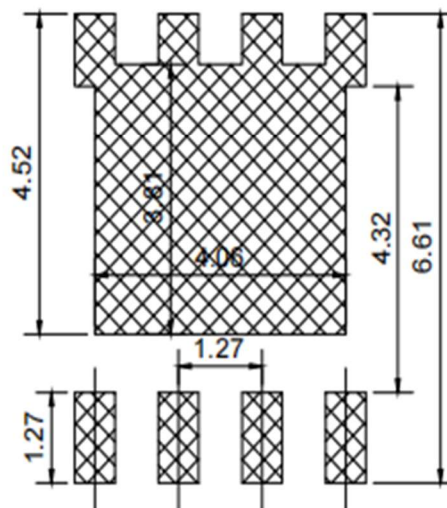


● Package Outline

1	WIP0D008	DFN5*6 SINGLE PACKAGE OUTLINE SPEC
REV	DRAWING NUMBER	TITLE



Land Pattern
(Only for Reference)



SYMBOLS	COMMON	
	UNIT: mm	
	MIN.	MAX.
A	0.90	1.17
b	0.30	0.51
c	0.15	0.35
D	4.80	5.40
D1	4.00	4.40
D2	4.80	5.00
E	5.90	6.25
E1	5.65	5.85
E2	1.10	-
e	1.27BSC	
L	0.05	0.25
L1	0.28	0.65
L2	0.38	0.71
H	3.30	3.90

● Note

- ① Pulse : $V_{GS}=+20V/-20V$, Duty cycle=50%, $T_j=175^{\circ}C$, $t=1000$ hours; For DC , the following test conditions can be passed: $V_{GS}=+20V/-10V$, $T_j=175^{\circ}C$, $t=1000$ hours;
- ② Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate;
- ③ Practically the current will be limited by PCB, thermal design and operating temperature. $V_{GS}=10V$.

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● Revision History

Version	Date	Change
A	2022/1/6	New
B	2022/2/26	1.Add Dynamic characteristic t_f , t_r etc.
C	2022/9/5	1.Add Reach,HF figure,2.ID modify
D	2022/9/19	Change dimension A,L
E	2023/12/19	Correct SOA
F	2024/2/28	Correct package outline dimension
G	2024/8/30	Modified $R_{ds(on)}$ up limit, $i_d@75^{\circ}\text{C}, 100^{\circ}\text{C}$
H	2025/1/16	Correct SOA
H1	2025.7.23	1. Add 1us SOA curve 2. Add transient thermal impedance curve
I	2025/12/16	1. Apply new datasheet format. 2. Modify Q_g value and chart 3. Tighten V_{TH} upper limit